CLAIMS

1. A semiconductor apparatus containing a low potential reference circuit region and a high potential reference circuit region between which signals are transmitted, the semiconductor apparatus comprising:

a high withstand voltage separating region arranged between the low and high potential reference circuit regions;

a relay semiconductor device for transmitting a signal from one of the low and high potential reference circuit regions to the other of them; and

an insulating partition arranged between at least one of the low and high potential reference circuit regions and the relay semiconductor device, the insulating partition being filled with insulating material in a trench,

wherein output wiring of the relay semiconductor device is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

2. A semiconductor apparatus according to claim 1 further comprising a substrate region arranged below the low and high potential reference circuit regions, wherein

bottom portion of the insulating partition extends to the substrate region, and

the insulation partition surrounds the relay semiconductor device.

3. A semiconductor apparatus according to claim 1 or claim 2 further comprising a group of insulating partitions arranged between the low and high potential reference circuit regions, the group of insulating

partitions dividing space between the low and high potential reference circuit regions into plural regions.

4. A semiconductor apparatus containing a low potential reference circuit region and a high potential reference circuit region between which signals are transmitted, the semiconductor apparatus comprising relay semiconductor devices for transmitting signals between the low and high potential reference circuit regions, each relay semiconductor device being surrounded with an insulating partition filled with insulating material in a trench, wherein

the relay semiconductor devices are arranged to form a ring shape which separates the low and high potential reference circuit regions, and

output wiring of each relay semiconductor device is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

5. A semiconductor apparatus according to claim 1 or claim 4 further comprising:

a substrate region arranged below the low and high potential reference circuit regions; and

an insulating layer embedded between the low and high potential reference circuit regions and the substrate region, the insulating layer electrically insulating the low and high potential reference circuit regions from the substrate region,

wherein bottom portions of the insulating partitions extend to the insulating layer and the insulation partitions surround the relay semiconductor devices.

6. A semiconductor apparatus comprising:

a semiconductor substrate of first conduction type;

a first region of second conduction type formed above the semiconductor substrate, the first region constituting a low potential reference circuit region;

a second region of second conduction type formed above the semiconductor substrate apart from the first region, the second region constituting a high potential reference circuit region;

a third region arranged between the first and second regions, formed in a ring shape surrounding one of the first and second regions, the third region constituting a high withstand voltage terminal region;

a fourth region arranged forming an incorporated ring structure together with the third region, the fourth region constituting a relay semiconductor device region for transmitting a signal between the first and second regions; and

an insulating partition arranged between at least one of the first and second regions and the fourth region, the insulating partition being filled with insulating material in a trench,

wherein output wiring of a relay semiconductor device in the fourth region is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

7. A semiconductor apparatus comprising:

a semiconductor substrate of either first or second conduction type;

an insulating film formed on the semiconductor substrate;

a first region of second conduction type formed on the insulating

film, the first region constituting a low potential reference circuit region;

a second region of second conduction type formed on the insulating film apart from the first region, the second region constituting a high potential reference circuit region;

a third region arranged between the first and second regions, formed in a ring shape surrounding one of the first and second regions, the third region constituting a high withstand voltage terminal region;

a fourth region arranged forming an incorporated ring structure together with the third region, the fourth region constituting a relay semiconductor device region for transmitting a signal between the first and second regions; and

an insulating partition arranged between at least one of the first and second regions and the fourth region, the insulating partition being filled with insulating material in a trench,

wherein output wiring of a relay semiconductor device in the fourth region is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

8. A semiconductor apparatus according to claim 6 or claim 7, wherein

bottom portion of the insulating partition extends to either the semiconductor substrate or the insulating film, and

the insulating partition surrounds periphery of a relay semiconductor device in the fourth region from at least three directions.

9. A semiconductor apparatus according to claim 6 or claim 7, wherein the third region composes junction isolation type structure in which high withstand voltage is maintained by PN junction.

10. A semiconductor apparatus according to claim 6 or claim 7, wherein the third region has insulation isolation type structure in which high withstand voltage is maintained by a plurality of insulating partitions.

11. A semiconductor apparatus according to claim 10, wherein

regions partitioned by the insulating partitions have capacitor structure in which the insulating partitions works as dielectric film, and

potential elevates gradually from the first region side toward the second region side.

12. A semiconductor apparatus comprising:

a semiconductor substrate of first conduction type;

a first region of second conduction type formed above the semiconductor substrate, the first region constituting a low potential reference circuit region;

a second region of second conduction type formed above the semiconductor substrate apart from the first region, the second region constituting a high potential reference circuit region;

a plurality of fourth regions arranged between the first and second regions, formed in a ring shape surrounding one of the first and second regions, the fourth regions constituting relay semiconductor device regions for transmitting signals between the first and second regions; and

an insulating partition arranged between at least one of the first and second regions and the fourth regions, the insulating partition being filled with insulating material in a trench,

wherein output wiring of a relay semiconductor device in a fourth region is wired to an output one of the low and high potential reference circuit region bridging over the insulating partition.

13. A semiconductor apparatus comprising:

a semiconductor substrate of either first or second conduction type;

an insulating film formed on the semiconductor substrate;

a first region of second conduction type formed on the insulating film, the first region constituting a low potential reference circuit region;

a second region of second conduction type formed on the insulating film apart from the first region, the second region constituting a high potential reference circuit region;

a plurality of fourth regions arranged between the first and second regions, formed in a ring shape surrounding one of the first and second regions, the fourth regions constituting relay semiconductor device regions for transmitting signals between the first and second regions; and

an insulating partition arranged between at least one of the first and second regions and the fourth regions, the insulating partition being filled with insulating material in a trench,

wherein output wiring of a relay semiconductor device in a fourth region is wired to an output one of the low and high potential reference circuit region bridging over the insulating partition.

14. A semiconductor apparatus according to claim 12 or claim 13, wherein

bottom portion of the insulating partition extends to either the semiconductor substrate or the insulating film, and

the insulating partition surrounds periphery of a relay semiconductor device in a fourth region from at least three directions.